CHRISTOPHER P. MAIORANA, P.C.

21643 East Nine Mile Rd., Suite A
St. Clair Shores, Michigan 48080

Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No. 0325.00278
Date: November 9, 1999

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): I-Teh Sha, Kuang-Yu Chen and Albert Chen

For: CIRCUIT AND METHOD FOR CONTROLLING A SPREAD SPECTRUM TRANSITION

Enclosed are:

1. X Specification (17 pages); Claims (6 pages); Abstract (1 page)

2. X 8 sheets of informal drawings.

3. X Oath or Declaration Total Pages 3
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$760.00
Total Claims	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $760.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ..... $ ____

X Assignment Recordal Fee ($40.00) ..... $ 40.00

TOTAL $800.00

X A check in the amount of $800.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

Correspondence Address:

Customer Number or Bar Code Label: 021363

PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL417952956US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on November 9, 1999.

By: Mary Donna Berkley
Mary Donna Berkley

Respectfully submitted,

By Robert M. Miller

Date: November 9, 1999

Robert M. Miller
Reg. No. 42,892
CHRISTOPHER P. MAIORANA, P.C.
21643 East Nine Mile Rd., Suite A
St. Clair Shores, Michigan 48080
(810) 498-0670

Attorney Docket No.: 0325.00278

0325.00278
IC99001

CIRCUIT AND METHOD FOR CONTROLLING A SPREAD SPECTRUM TRANSITION

Cross-Reference to Related Applications

The present invention may relate to co-pending application Attorney Docket No. 0325.00279, filed concurrently, which is hereby incorporated by reference in its entirety.

Field of the Invention

The present invention relates to spread spectrum clock generators generally and, more particularly, to a circuit and method for controlling a spread spectrum transition.

Background of the Invention

Electronic devices must meet maximum electromagnetic interference (EMI) radiation limits as specified by the U.S. FCC and other comparable regulatory agencies in other countries. New FCC requirements call for PC motherboards to be able to pass EMI tests "open box," so manufacturers will not be able to rely on the shielding provided by the case in meeting EMI requirements.

An EMI suppression-enabled clock IC can reduce the system radiated EMI. The reduction in radiated EMI can result in dramatic cost savings for the system. Conventional techniques for reducing EMI include ground planes, filtering components, shielding, and spread spectrum modulated system clocks.

In the spread spectrum technique, instead of concentrating all of a frequency reference's energy on a single frequency, the energy is spread out by modulating the frequency. The modulation results in the energy being spread over a frequency range, instead of being concentrated on one particular frequency. Since the FCC and other regulatory bodies are concerned with peak emissions, not average emissions, the reduction in peak energy due to spread spectrum modulation will help a product meet FCC requirements.

One type of spread spectrum modulation is center modulation (e.g., +/-). A center modulated clock provides the same system processing performance as for a CPU using a non-modulated clock. However, system designers are concerned about overboosting processors. If a processor designed for a 100 MHz reference is used with a reference that spends most of the time at 100.5 MHz, the processor will be operating at a higher than rated speed during

that period of time. To alleviate this concern, modulation can be specified as "down only," e.g., -0.5%. A -0.5% modulation, in the same 100 MHz example, would vary the frequency from 99.5 to 100 MHz. This is achieved by moving the center frequency down. What is specified as "100 MHz, with -0.5% modulation" can really be thought of as "99.75MHz with +/-0.25% modulation." Using "down only" modulation results in a performance degradation of a CPU, as the nominal 100 MHz signal is now less than 100MHz.

If the spread spectrum clock generator could be configured for the spread spectrum modulation to be switched on and off, a system could have reduced EMI while still providing top performance when needed. However, during the transition period when the spread spectrum modulation is switching on or switching off, the frequency can undershoot or overshoot the rated input frequency range of the CPU. When the undershoot or overshoot exceeds the clock input frequency range of the processor, tracking loss and hanging can result.

Referring to FIG.1, a block diagram of a circuit 10 illustrating a conventional phase lock loop based spread spectrum clock generator is shown. The circuit 10 generates a signal OUT in response to (i) a reference signal REF and a command signal SSON.

The signal REF is presented to an input prescaler 12 and a multiplexer 14. The signal OUT is presented to a feedback prescaler 20 and a multiplexer 22. The signal SSON is presented to (i) the control inputs of the multiplexers 14 and 20 and (ii) the spread spectrum circuitry 26. In response to the command signal SSON, (i) the multiplexer 14 selects between the reference signal REF and an output of the input prescaler 12, (ii) the multiplexer 22 selects between the output signal OUT and an output of the feedback prescaler 20 and (iii) the spread spectrum circuitry modulates the signal out.

Referring to FIG. 2, a timing diagram and an oscilloscope tracing illustrating signals of the circuit 10 are shown. The timing diagram illustrates that a transition 30 in the signal SSON results in an immediate transition at the control inputs of the multiplexers 14 and 20. A portion 40 of the oscilloscope tracing illustrates the large transient response of the circuit 10 when spread spectrum modulation is switched on.

Summary of the Invention

The present invention concerns a circuit and method for controlling a spread spectrum transition comprising a first circuit

and a second circuit. The first circuit may be configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal. The second circuit may be configured to synchronize said command signal to a feedback signal. The sequence of spread spectrum ROM codes may be generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

The objects, features and advantages of the present invention include providing a circuit and method that may (i) reduce overshoot and/or undershoot in the transient response of a spread spectrum clock generator, (ii) provide for synchronization of dividers and prescalers, and (iii) use a computer program to determine transient and steady-state spread spectrum behavior of a spread spectrum device.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram illustrating a conventional spread spectrum clock generator circuit;

FIG. 2 is a timing diagram and an oscilloscope trace illustrating various signals of the conventional spread spectrum clock generator of FIG. 1;

FIG. 3 is a block diagram illustrating a spread spectrum clock generator circuit in accordance with a preferred embodiment of the present invention;

FIG. 4 is a more detailed block diagram illustrating a preferred embodiment of the present invention;

FIG. 5 is a more detailed diagram of the PLL circuit of FIG. 4;

FIG. 6 is a timing diagram and an oscilloscope trace of various signals of the circuit of FIG. 4;

FIG. 7 is a diagram illustrating criteria used in determining when a sequence of spread spectrum ROM codes may be optimized;

FIG. 8 is a flow chart illustrating a process for optimizing a sequence of spread spectrum ROM codes in accordance with a preferred embodiment of the present invention; and

FIG. 9 is a diagram illustrating the optimization of a spread spectrum ROM code sequence.

Detailed Description of the Preferred Embodiments

Referring to FIG. 3, a block diagram of a circuit 100 is shown in accordance with a preferred embodiment of the present invention. The circuit 100 may be implemented, in one example, as a spread spectrum clock generator circuit. The circuit 100 may have a clock input 102, a control input 104, and an output 106. A reference signal (e.g., REF) is generally presented to the input 102. A command signal (e.g., SSON) is generally presented to the input 104. The circuit 100 may be configured to generate a clock signal (e.g., CLK) at the output 106 in response to (i) the signal REF and (ii) the signal SSON. When the signal SSON is in a first state (e.g., a logic "0", or LOW), the signal CLK may be an unmodulated clock signal. When the signal SSON is in a second state (e.g., a logic "1", or HIGH), the signal CLK may be a spread spectrum modulated clock signal. The particular polarity of the signal SSON may be changed to meet the design criteria of a particular application. The signal CLK may be presented, in one

example, to a clock input 108 of a CPU/Motherboard (or other device requiring a clock input) 110.

The circuit 100 generally comprises a circuit 112 and a circuit 114. The circuit 112 may be, in one example, a synchronizer circuit. The circuit 114 may be, in one example, a modulator circuit. The signal SSON is generally presented at an input 115 of the circuit 112. A feedback signal (e.g., FDBCK) is generally presented at an input 116 of the circuit 112. In one example, the circuit 112 may be configured to generate (i) a first control signal (e.g., SSON_A) at an output 118 and (ii) a second control signal (e.g., SSON_B) at an output 120 in response to (i) the signal SSON and (ii) the signal FDBCK.

The circuit 114 may have an input 122, an input 124, an input 125, and an output 126. The circuit 114 may be configured to receive the signal REF from the input 102. The signal SSON_A is generally presented to the input 122. The signal SSON_B is generally presented to the input 124. The signal SSON is generally presented to the input 125. The circuit 114 may be configured to generate (i) the signal FDBCK at the output 126 and (ii) the signal CLK in response to (a) the signal REF, (b) the signal SSON_A, (c)

the signal SSON_B, and (d) the signal SSON. The signal FDBCK may be used as a control signal.

Referring to FIG. 4, a more detailed block diagram of the circuit 100 is shown. The circuit 112 generally comprises, in one example, a latch 128 and a latch 130. The signal SSON is generally presented at an input 132 of the latch 128 and an input 134 of the latch 130. The signal FDBCK is generally presented to a control input 136 of the latch 128 and a control input 138 of the latch 130. The signal SSON_A is generally presented by the latch 128 in response to (i) the signal SSON and (ii) the signal FDBCK. The signal SSON_B is generally presented by the latch 130 in response to (i) the signal SSON and (ii) the signal FDBCK. In an alternative embodiment (not shown), the circuit 112 may comprise a single latch. In the example of a single latch, the signal SSON_A and the signal SSON_B may be the same signal.

The circuit 114 generally comprises, in one example, an input prescaler 140, a multiplexer 142, an input divider 144, a phase lock loop (PLL) 146, a feedback prescaler 148, a multiplexer 150, a feedback divider 152, a spread spectrum circuit 154, and a ROM 156. The signal REF is generally presented to an input 158 of the input prescaler 140 and an input 160 of the multiplexer 142.

An output 162 of the input prescaler 140 is generally connected to an input 164 of the multiplexer 142. The signal SSON_A is generally presented to a control input 166 of the multiplexer 142. An output 168 of the multiplexer 142 is generally connected to an input 170 of the input divider 144. An output 172 of the input divider 144 is generally connected to an input 174 of the PLL 146. The signal FDBCK is generally presented to an input 176 of the input divider 144. The PLL 146 may be configured to generate the signal CLK.

The signal CLK is generally presented to an input 178 of the feedback prescaler 148 and an input 180 of the multiplexer 150. An output 182 of the feedback prescaler 148 is generally connected to an input 184 of the multiplexer 150. The signal SSON_B is generally presented at a control input 186 of the multiplexer 150. An output 188 of the multiplexer 150 is generally connected to a clock input 190 of the feedback divider 152. The feedback divider 152 may be configured to generate the signal FDBCK.

The signal FDBCK is generally presented to an input 192 of the spread spectrum circuit 154. The signal SSON is generally presented to an input 193 of the spread spectrum circuit 154. An output 194 of the spread spectrum circuit 154 is generally

connected to an input 196 of the feedback divider 152. A sequence of spread spectrum ROM codes from the ROM 156 may be presented, in one example, at an input 198 of the spread spectrum circuit 154. However, other connections between the spread spectrum circuit 154 and the ROM 156 may be implemented accordingly to meet the design criteria of a particular application. The spread spectrum circuit 154 may be configured to control the feedback divider 152 in response to the sequence of spread spectrum ROM codes.

Referring to FIG. 5, a more detailed diagram of the PLL 146 of FIG. 4 is shown. The PLL 146 may comprise a phase frequency detector (PFD) 200, a charge pump 202, a voltage controlled oscillator (VCO) 204, a capacitor 206, a capacitor 208, and a resistor 210. A reference signal (e.g., U) is generally presented to a first input of the PFD 200. The signal FDBCK is generally presented to a second input of the PFD 200. The PFD 200 may be configured, in one example, to generate a pump signal (e.g., PUMP) in response to (i) the signal U and (ii) the signal FDBCK.

The signal PUMP is generally presented, in one example, to an input of the charge pump 202. The charge pump 202 may be configured to generate a control signal (e.g., CP) in response to the signal PUMP. The signal CP may be a current signal. The

signal CP is generally presented to a node formed by (i) an input of the VCO 204, (ii) a first terminal of the capacitor 206, and (iii) a first terminal of the resistor 210. A second terminal of the capacitor 206 is generally connected to a ground potential. A second terminal of the resistor 210 is connected to a first terminal of the capacitor 208. A second terminal of the capacitor 208 is generally connected to the ground potential. The VCO 204 may be configured to generate the signal CLK in response to the signal CP.

In the present invention, the switching on or switching off of spread spectrum modulation is generally synchronized to the signal FDBCK. The selection between a signal and a prescaled version of the signal by the multiplexers 142 and 150 may be synchronized with the updating of the feedback divider. The feedback divider may be controlled by the spread spectrum circuit 154 in response to an optimized sequence of spread spectrum ROM codes. The sequence of spread spectrum ROM codes may be optimized to reduce undershoot and overshoot of the frequency of the signal CLK during a spread spectrum transition. The process of optimization generally begins by generating the ROM codes according

to a predetermined mathematical formula. In a preferred embodiment, the following mathematical formula may be used:

$$\begin{bmatrix} X1(N+1) \\ X2(N+1) \\ X3(N+1) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{VCO}{FBD(N+1)} & 0 \\ \frac{CP(N+1)}{C1} & -\frac{1}{C1 \cdot R1} & -\frac{1}{C1 \cdot R1} \\ 0 & \frac{1}{C2 \cdot R1} & -\frac{1}{C2 \cdot R1} \end{bmatrix} \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} U1(N+1) \\ U2(N+1) \\ U3(N+1) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix}$$

Reading the equation in connection with FIG. 4 and FIG. 5, the term VCO is generally the gain of the voltage controlled oscillator 204. C1 and C2 are generally the capacitance values of the capacitor 206 and the capacitor 208, respectively. R1 is generally the resistance value of the resistor 210. In one example, R1 may be 40KΩ when spread spectrum modulation is OFF and 24 KΩ when spread spectrum modulation is ON. The term FBD is generally the feedback divider value of feedback divider 152. The term Δt(N) is generally the time interval between the last time step and present time. U(N) is generally the reference signal presented to the input 174 of the PLL 146. The term CP(N) is generally the current from an output of the charge pump 202. The particular values of the various variables may be modified or optimized accordingly to meet the design criteria of a particular implementation. Additionally, the formula listed is one example of a formula that may be used to

generate ROM codes. Other formulas may be substituted in particular design applications.

When the generation of spread spectrum ROM codes is complete, the sequence of the spread spectrum ROM codes generated may be optimized by a process described below in connection with FIG. 7.

Referring to FIG. 6, a timing diagram and an oscilloscope trace illustrating various signals of the circuit 100 is shown. In the timing diagram, a transition 220 in the signal SSON is synchronized with a transition 222 in the signal FDBCK to generate the transitions 224 and 226 in the signals SSON_A and SSON_B, respectively. Simulation and measured examples of the signal CLK illustrating the spread spectrum transient behaviors as generally controlled by the present invention are also shown.

Referring to FIG. 7, a waveform diagram illustrating the criteria for determining whether spread spectrum transient behavior is good (e.g., within acceptable design tolerances) or bad (e.g., not within acceptable design tolerances) is shown. A value foff is generally the unmodulated frequency of the signal CLK. A value fmax is generally the maximum frequency of the signal CLK when spread spectrum modulation is on. A value fmin is generally the

minimum frequency of the signal CLK when spread spectrum modulation is on. A function f(t) generally represents the changes in the frequency of the signal CLK during the transition time period. A value Δf generally represents the peak to peak frequency range of the signal CLK when spread spectrum modulation is on. The sequence of the spread spectrum ROM codes is generally considered optimized when the function f(t) is greater than or substantially equal to the value fmin and less than or substantially equal to the value foff.

Referring to FIG. 8, a flow chart illustrating a process for optimizing the sequence of spread spectrum ROM codes is shown. The process may be performed, in one example, using a computer program to simulate the transient and steady-state spread spectrum behavior of the circuit 100.

The circuit 100 is generally initialized at power supply ramping (e.g., block 300). The circuit 100 is generally allowed to reach a steady-state condition with the signal SSON in an unasserted state indicating no modulation (e.g., block 310). The sequence of spread spectrum ROM codes, generated as described above, is generally loaded (e.g., block 320).

The signal SSON is generally asserted to begin spread spectrum modulation (e.g., block 330). The circuit 100 is generally allowed to move (i) from a steady-state condition with no modulation, (ii) through spread spectrum start-up transient behavior (e.g., block 340), and (iii) into a steady-state condition with spread spectrum modulation on (e.g., block 350).

When the circuit 100 has reached the steady-state with spread spectrum modulation on, the signal SSON is generally de-asserted (e.g., block 360). The circuit 100 is then allowed to move (i) from the steady-state condition with modulation on, (ii) through spread spectrum turn off transient behavior (e.g., block 370), and (iii) to a steady-state condition with no modulation of the signal CLK (e.g., block 380).

The frequency changes of the signal CLK (e.g., f(t)) during the transition periods are compared with predetermined criteria (e.g., block 390). The comparison determines, whether or not, the frequency was (i) below the predetermined minimum value (e.g., fmin) or (ii) above the frequency of the signal CLK with no modulation (e.g., foff).

If the frequency changes of the signal CLK did not exceed the range (e.g., fmin $\leq$ f(t) $\leq$ foff), the sequence of ROM codes is

generally considered optimized (e.g., block 400). If the frequency changes of the signal CLK were outside the predetermined range (e.g., f(t) < fmin or f(t) > foff), the sequence of spread spectrum ROM codes is generally shifted one position (e.g., block 410). The process may be repeated until the predetermined criteria are met (e.g., blocks 330-410).

Referring to FIG. 9, a more detailed block diagram of the ROM 156 illustrating the process of shifting the spread spectrum ROM code, as mentioned in the block 410 of FIG. 8, is shown. If the criteria for the transient response have not been met, the feedback divider value in the last address location 400n of the spread spectrum ROM 156 is generally moved to the first address location 400a. All other values in the ROM 156 are generally shifted to the next location.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. An apparatus comprising:

a first circuit configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal; and

a second circuit configured to synchronize said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

2. The apparatus according to claim 1, wherein said apparatus comprises a spread spectrum clock generator circuit, wherein said clock signal is spread spectrum modulated.

3. The apparatus according to claim 2, wherein said spread spectrum modulation of said clock signal can be switched on and off in response to said command signal.

4. The apparatus according to claim 2, wherein said circuit is used with a motherboard or CPU.

5. The apparatus according to claim 1, wherein said second circuit is further configured to generate one or more control signals in response to (i) said command signal and (ii) said feedback signal.

6. The apparatus according to claim 5, wherein said second circuit comprises a first latch.

7. The apparatus according to claim 6, wherein said second circuit further comprises a second latch.

8. The apparatus according to claim 3, wherein said predetermined criteria are applied to said clock signal during a transition period when spread spectrum modulation is switching on or switching off.

9. The apparatus according to claim 1, wherein said predetermined criteria includes a predetermined minimum frequency for said clock signal.

10. The apparatus according to claim 7, wherein said predetermined criteria further includes a predetermined maximum frequency for said clock signal.

11. The apparatus according to claim 1, wherein said predetermined mathematical formula is:

$$\begin{bmatrix} X1(N+1) \\ X2(N+1) \\ X3(N+1) \end{bmatrix} = \begin{bmatrix} 0 & -\frac{VCO}{FBD(N+1)} & 0 \\ \frac{CP(N+1)}{C1} & -\frac{1}{C1 \cdot R1} & -\frac{1}{C1 \cdot R1} \\ 0 & \frac{1}{C2 \cdot R1} & -\frac{1}{C2 \cdot R1} \end{bmatrix} \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} U1(N+1) \\ U2(N+1) \\ U3(N+1) \end{bmatrix} * \Delta t(N) + \begin{bmatrix} X1(N) \\ X2(N) \\ X3(N) \end{bmatrix}$$

12. The apparatus according to claim 1, wherein:

said sequence of spread spectrum ROM codes is optimized using a computer program to simulate transient behavior of said apparatus.

13. An apparatus comprising:

means for generating a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes and (iii) a command signal; and

means for synchronizing said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes was

generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

14. A method for controlling a spread spectrum transition comprising the steps of:

generating a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes and (iii) a command signal; and

synchronizing said command signal to a feedback signal, wherein said sequence of spread spectrum ROM codes is generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

15. The method according to claim 14, wherein the step of generating said sequence of spread spectrum ROM codes further comprises the sub-steps of:

(A) selecting a number of ROM codes to be used to generate a spread spectrum modulation signal; and

(B) generating said number of ROM codes according to said predetermined mathematical formula.

16. The method according to claim 15, wherein the step of optimizing said sequence of spread spectrum ROM codes further comprises the sub-steps of:

(A) initializing a phase lock loop (PLL) at power supply ramping;

(B) stabilizing said PLL with spread spectrum modulation turned off;

(C) loading said sequence of spread spectrum ROM codes;

(D) switching on spread spectrum modulation;

(E) recording transient behavior of said clock signal until PLL is in spread spectrum steady-state;

(F) switching off spread spectrum modulation;

(G) recording transient behavior of said clock signal until spread spectrum modulation is completely off;

(H) comparing recorded transient behavior to predetermined criteria;

(I) if the recorded transient behavior does not meet said predetermined criteria, shifting said sequence of spread spectrum ROM codes, wherein a last ROM code is moved to a first position and remaining ROM codes are shifted one position forward;

(J) if the recorded transient behavior meets said predetermined criteria, finalizing said sequence of spread spectrum ROM codes; and

(K) repeating sub-steps (D) through (J) until said recorded transient response meets said predetermined criteria.

17. The method according to claim 16, wherein said sub-steps are performed by a computer program.

18. The method according to claim 14, wherein said step of generating said clock signal further comprises the sub-step of controlling a feedback divider with said sequence of spread spectrum ROM codes.

19. The method according to claim 14, wherein the step of synchronizing said command signal to said feedback signal further comprises generating one or more control signals in response to (i) said command signal and (ii) said feedback signal.

20. The method according to claim 19, wherein one or more latches are used.

ABSTRACT OF THE DISCLOSURE

A circuit and method for controlling a spread spectrum transition are presented comprising a first circuit and a second circuit. The first circuit may be configured to generate a clock signal in response to (i) a reference signal, (ii) a sequence of spread spectrum ROM codes, and (iii) a command signal. The second circuit may be configured to synchronize said command signal to a feedback signal. The sequence of spread spectrum ROM codes may be generated according to a predetermined mathematical formula and optimized in accordance with predetermined criteria.

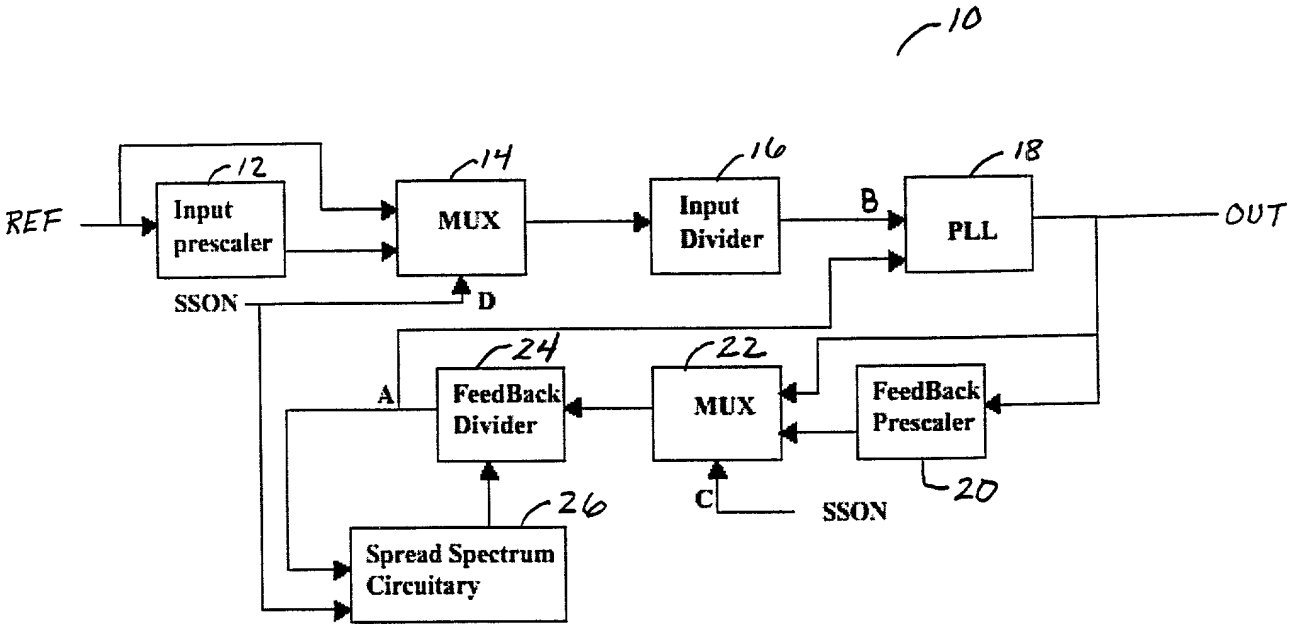

10
REF
12
Input prescaler
14
MUX
16
Input Divider
B
18
PLL
OUT
SSON
D
24
A
FeedBack Divider
22
MUX
FeedBack Prescaler
20
C
SSON
26
Spread Spectrum Circuitary

FIG.1

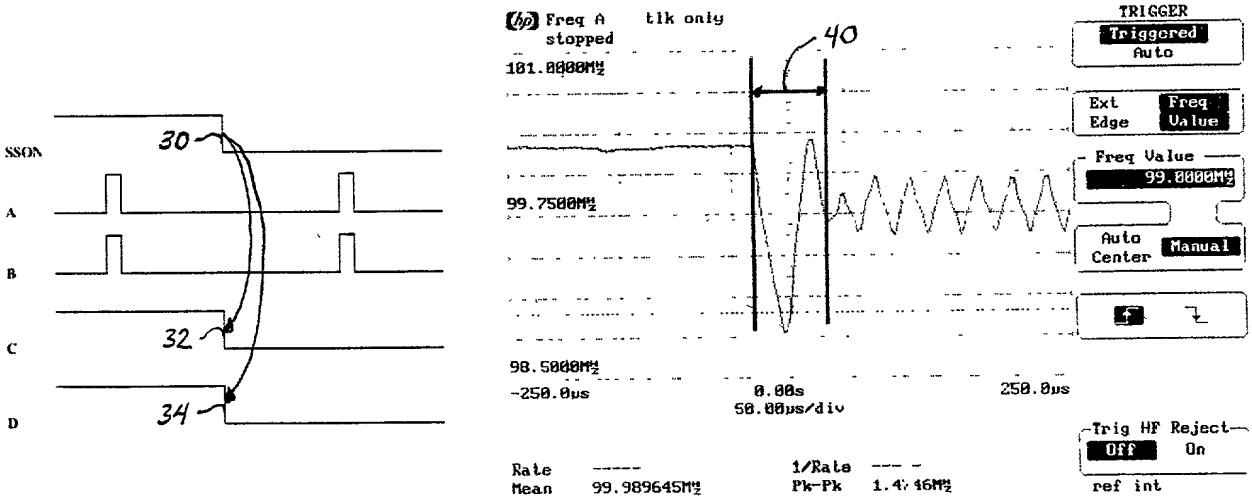

SSON
30
A
B
C
32
D
34
Freq A stopped
tlk only
101.0000MHz
40
99.7500MHz
98.5000MHz
-250.0µs
0.00s
50.00µs/div
250.0µs
TRIGGER
Triggered
Auto
Ext Edge
Freq Value
Freq Value
99.0000MHz
Auto Center
Manual
Trig HF Reject
Off
On
Rate -----
Mean 99.989645MHz
1/Rate ---
Pk-Pk 1.4?46MHz
ref int

FIG. 2

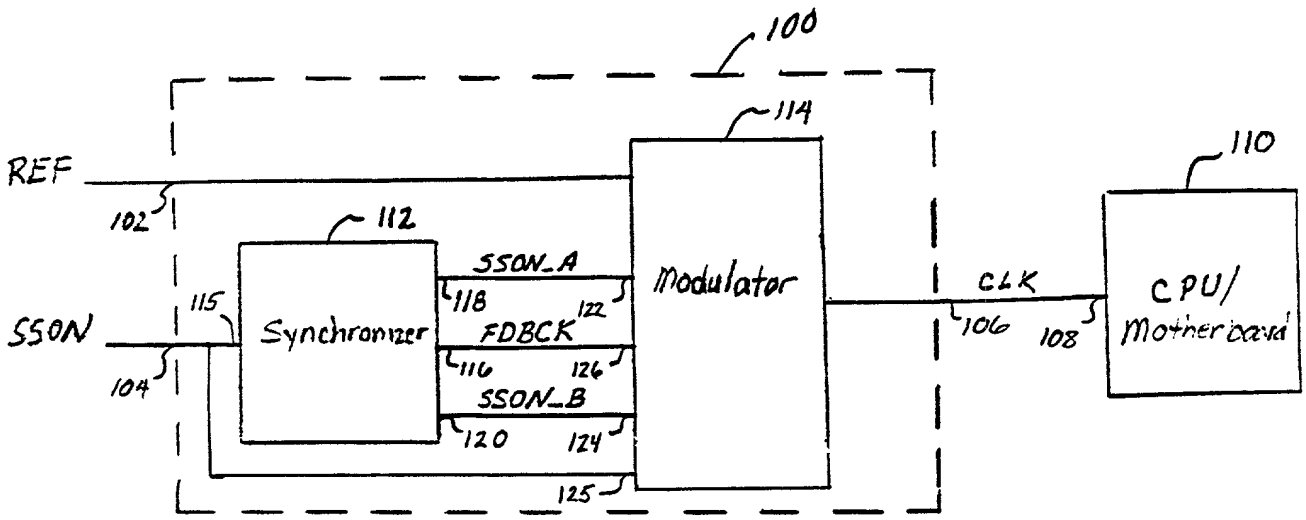

100
114
110
REF
102
112
SSON_A
118
122
Modulator
CLK
CPU/
Motherboard
SSON
115
Synchronizer
FDBCK
116
126
106
108
104
SSON_B
120
124
125

FIG.3

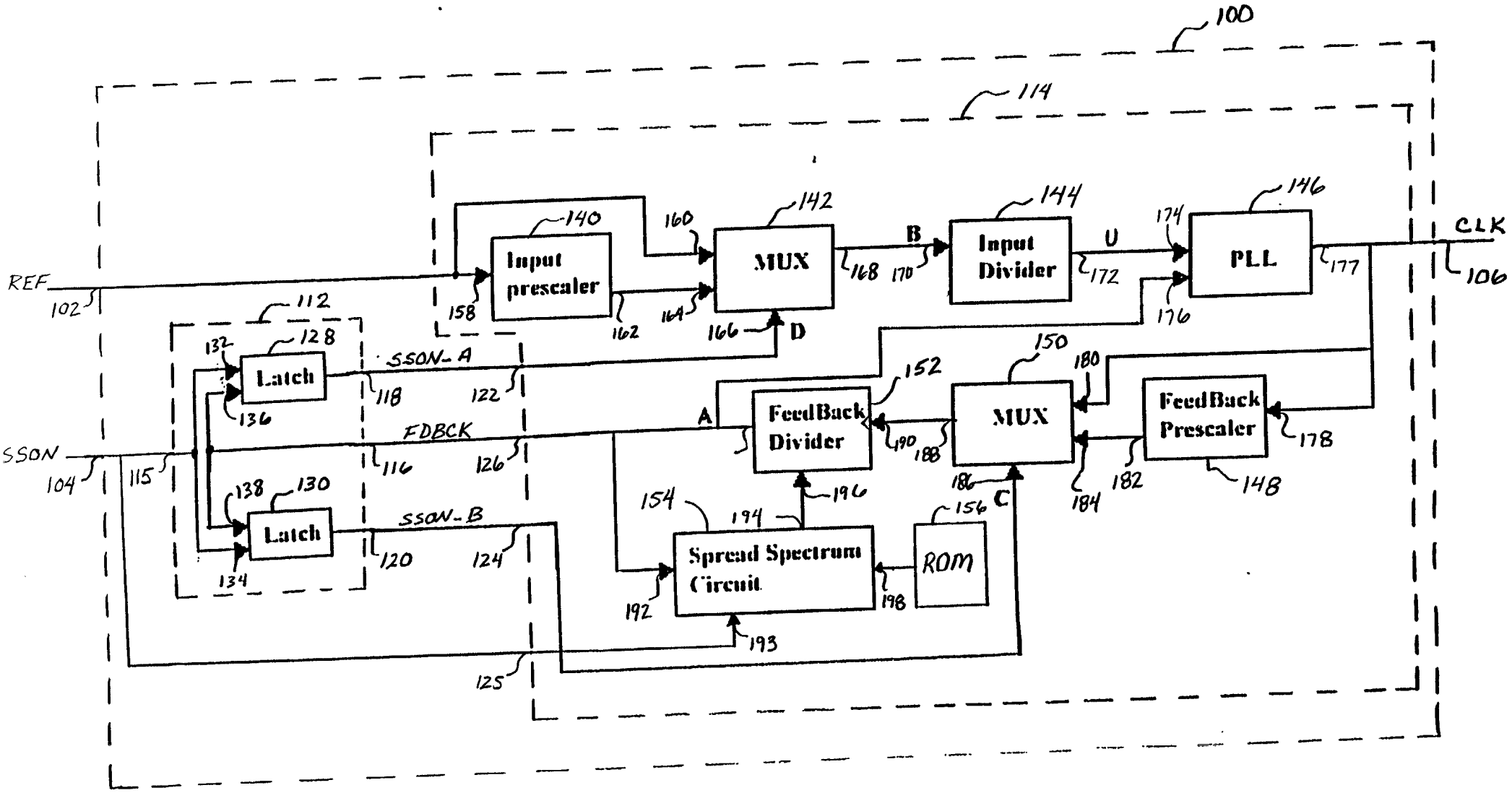

100
114
REF
102
112
158
Input prescaler
140
160
MUX
142
B
168
170
Input Divider
144
U
172
174
PLL
146
177
CLK
106
176
D
166
162
164
128
Latch
132
136
SSON_A
118
122
SSON
104
115
FDBCK
116
126
138
130
Latch
134
SSON_B
120
124
A
FeedBack Divider
152
190
188
MUX
150
180
FeedBack Prescaler
178
182
184
148
186
C
196
154
194
156
Spread Spectrum Circuit
ROM
192
198
193
125

FIG.4

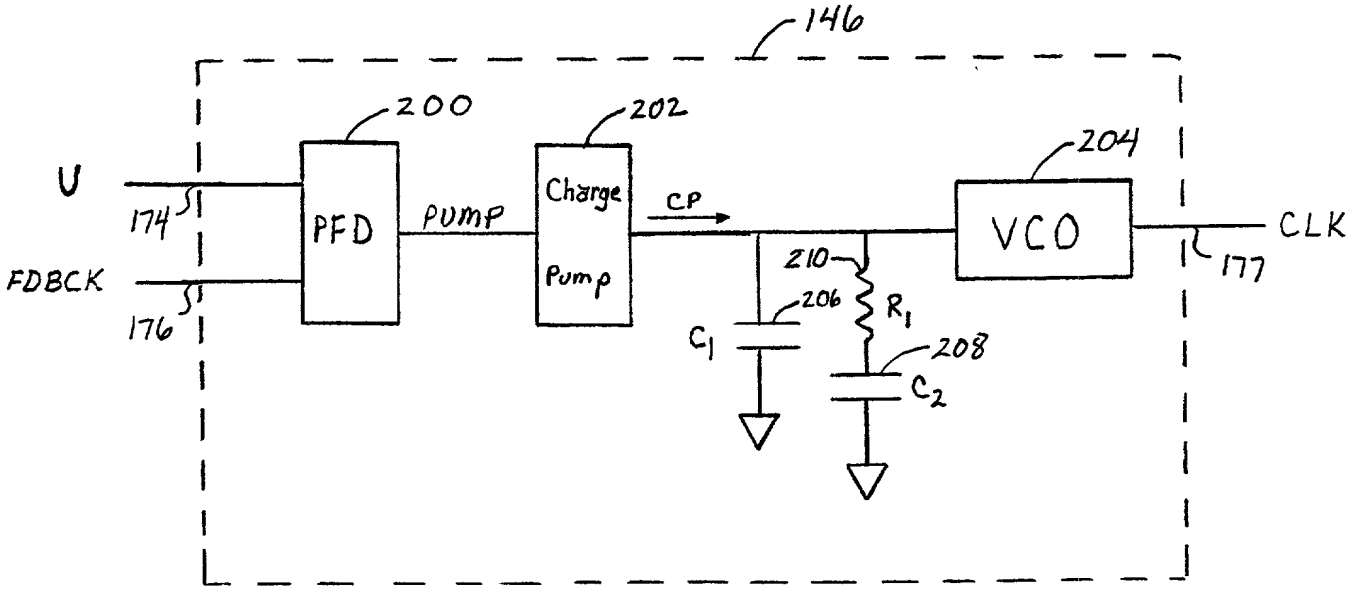
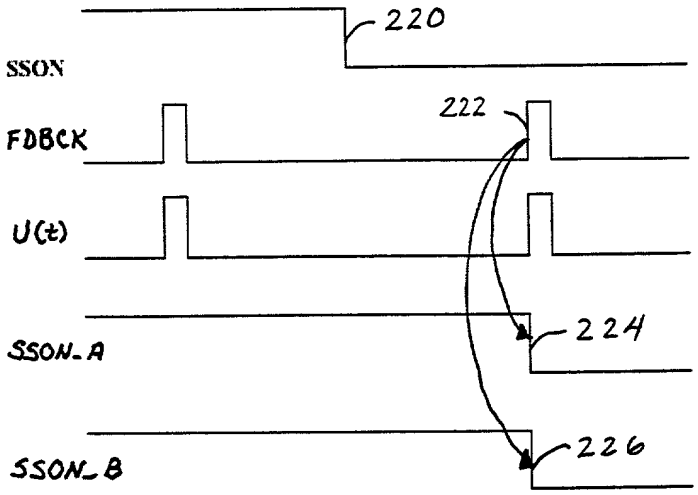
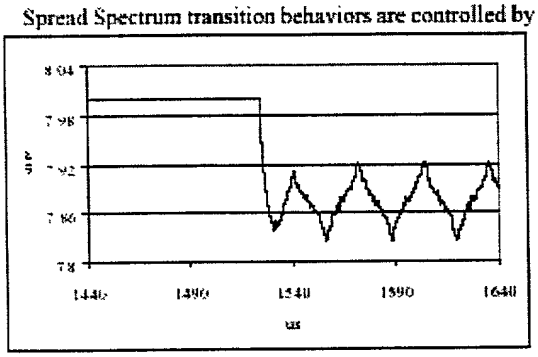

146
200
202
204
U
174
FDBCK
176
PFD
PUMP
Charge
Pump
CP
VCO
CLK
177
210
206
208
R_1
C_1
C_2

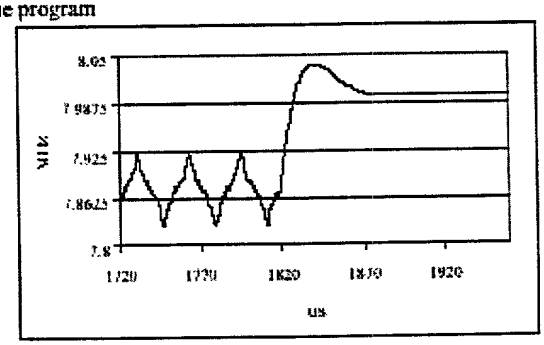
FIG.5



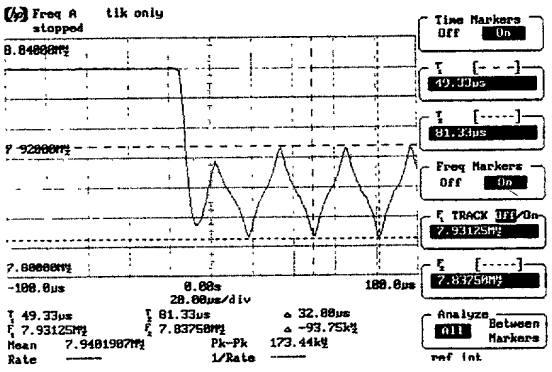
Spread Spectrum transition behaviors are controlled by the program



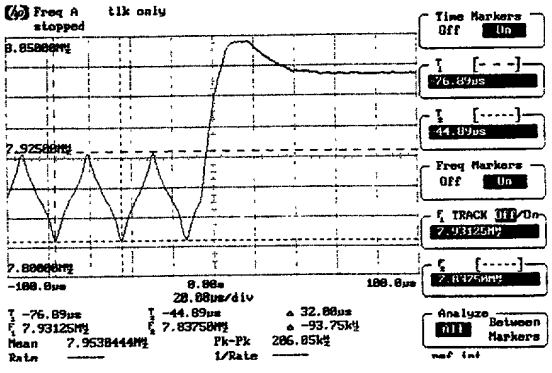
(a)



(a)



(b)



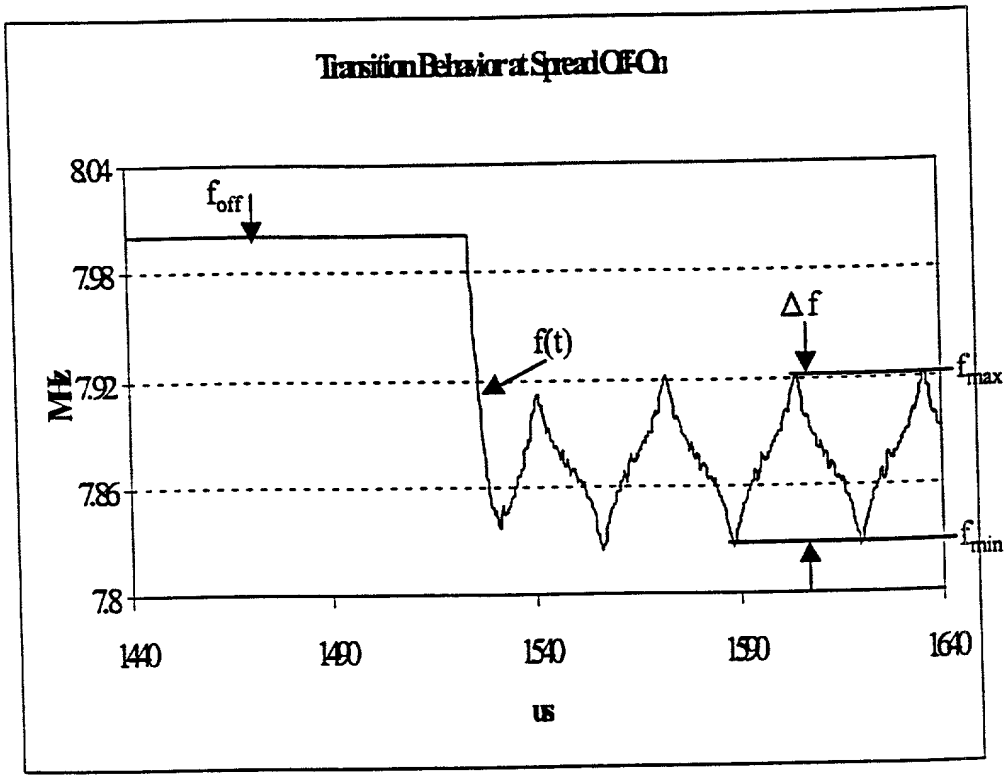
(b)

(a) Simulation (b) Measured results in off-on transition

(a) Simulation (b) Measured results in on-off transition

FIG. 6

Criteria for determining "good and bad" SS transient behavior



f(t): PLL's running frequency in transient period

f_{off}: PLL's SSCG off frequency

f_{max}: Maximum frequency in SSCG on

f_{min}: Minimum frequency in SSCG on

Δ f: Peak to peak frequency in SSCG

Criteria need to be satisfied:

Frequency running range during transient $f_{min} \leq f(t) \leq f_{off}$

FIG.7

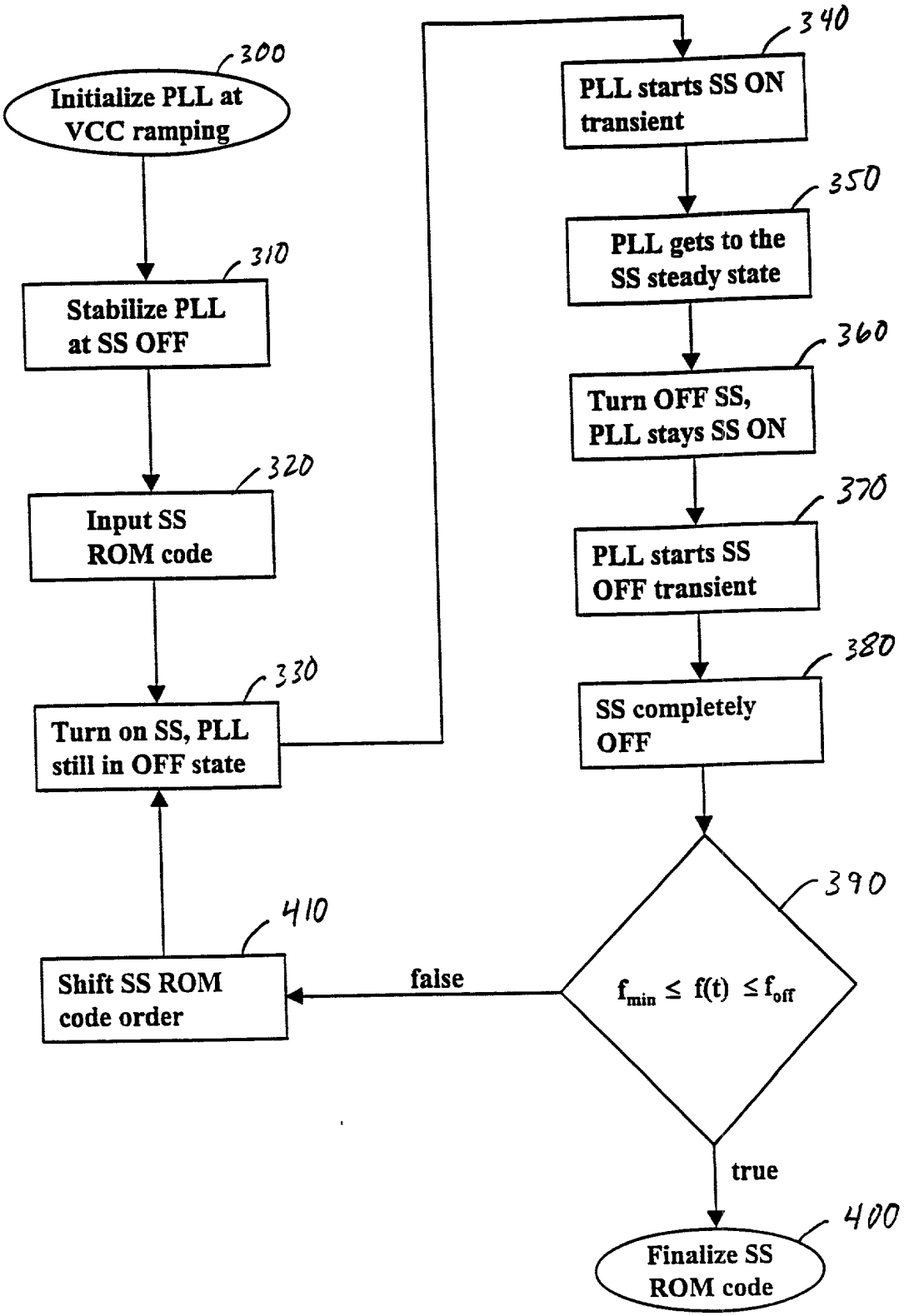
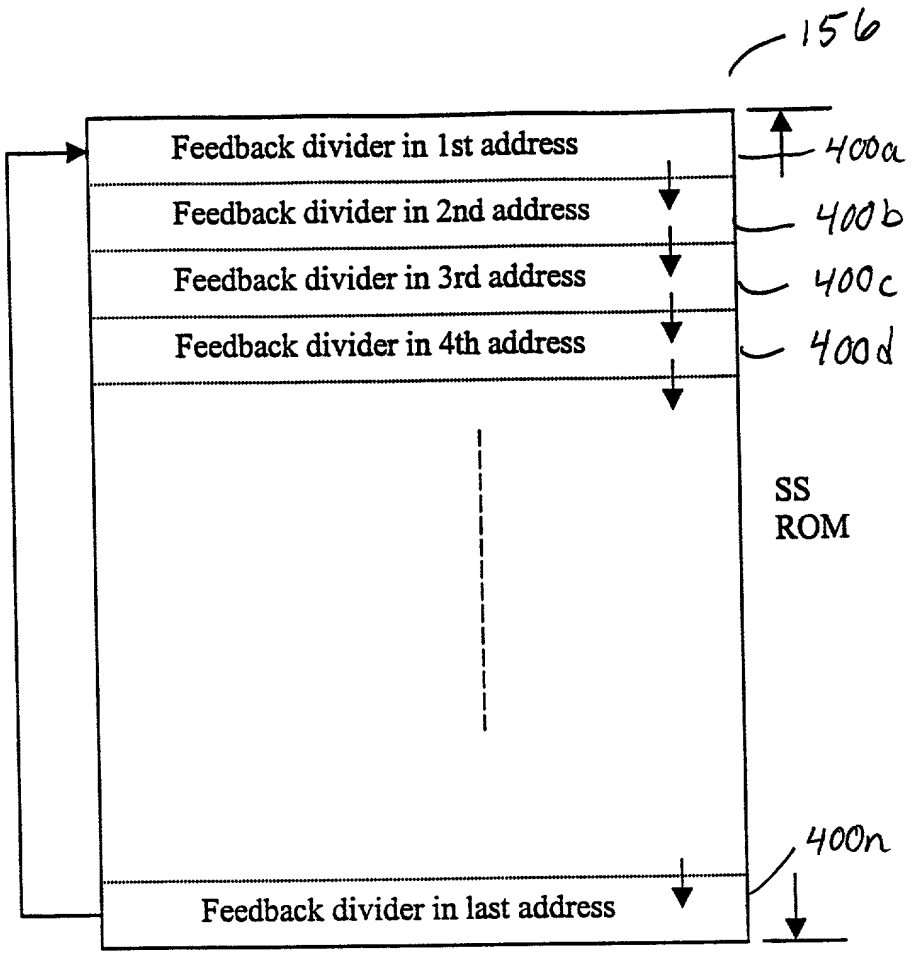

300
Initialize PLL at VCC ramping
310
Stabilize PLL at SS OFF
320
Input SS ROM code
330
Turn on SS, PLL still in OFF state
340
PLL starts SS ON transient
350
PLL gets to the SS steady state
360
Turn OFF SS, PLL stays SS ON
370
PLL starts SS OFF transient
380
SS completely OFF
390
$f_{min} \leq f(t) \leq f_{off}$
false
410
Shift SS ROM code order
true
400
Finalize SS ROM code

FIG.8

Order shifting step in response to bad behavior



Move feedback divider in last address to 1st address and shift down SS ROM code.

FIG.9

Docket No. 0325.00278

DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled "**CIRCUIT AND METHOD FOR CONTROLLING A SPREAD SPECTRUM TRANSITION**", which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

021363

PATENT TRADEMARK OFFICE

We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

I-Teh Sha
Name of First Joint Inventor

I-Teh Sha
Signature of First Joint Inventor

Nov 4, 1999
Date

Post Office Address:
1901 Halford Ave., Apt. 100
Santa Clara, CA 95051

Citizen of: Republic of China, Taiwan
Residence: 1901 Halford Ave., Apt. 100
Santa Clara, CA 95051

Kuang-Yu Chen
Name of Second Joint Inventor

K.-Y. Chen
Signature of Second Joint Inventor

Nov 4, 1999
Date

Post Office Address:
20489 Chalet Lane
Saratoga, CA 95070

Citizen of: United States of America
Residence: 20489 Chalet Lane
Saratoga, CA 95070

Albert Chen
Name of Third Joint Inventor

Albert Chen
Signature of Third Joint Inventor

Nov. 4 1999
Date

Post Office Address:
13091 River Ranch Circle
Saratoga, CA 95070

Citizen of: Republic of China, Taiwan
Residence: 13091 River Ranch Circle
Saratoga, CA 95070